

AMC Port Map Gap-Analysis

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1. PURPOSE

This document is the SCOPE AMC Port-map Gap Analysis. It was prepared by members of the SCOPE Alliance, consolidating their views of what properties are important in AMC-based MicroTCA and AdvancedTCA systems. It provides guidelines and narrows options, with the intention of facilitating the creation of interoperable open carrier-grade base platforms.

2. AUDIENCE

This document is intended for the following audiences:

- ✓ PICMG, other standardization bodies, and related trade associations, who may find the information in the Gap Analysis useful in defining new specifications or developing modifications to existing AMC-related specifications
- ✓ Telecommunications Equipment Manufacturers and others who use AMC technologies as the basis for building standards-based equipment
- ✓ System, board, and chip suppliers who build AMC subcomponents and AMC-based systems

This document assumes that the reader is familiar with the AMC.0, AMC.1, AMC.2, AMC.3, AMC.4, and MicroTCA.0 specifications at a detailed technical level.

3. REFERENCES

- 1) PICMG MicroTCA.0 Micro Telecommunications Computing Architecture Base Specification R1.0
- 2) PICMG AMC.0 Advanced Mezzanine Card Base Specification R2.0
- 3) PICMG AMC.1 PCI-Express and Advanced Switching on AdvancedMC R1.0
- 4) PICMG AMC.2 Ethernet Advanced Mezzanine Card Specification R1.0
- 5) PICMG AMC.3 Storage Advanced Mezzanine Card Specification R1.0
- 6) PICMG AMC.4 Serial RapidIO Advanced Mezzanine Card Specification

4. INTRODUCTION

The PICMG AMC.0 specification provides a framework definition for fabric port interconnect usage provided by AMC modules. Subsidiary specifications (referred to as “dot specs” e.g. AMC.1, AMC.2, etc.) were created to define the usage of ports for interconnects such as PCI-Express, Ethernet, SAS/SATA, and Serial RapidIO. Each of these dot-specs maps a particular fabric-type into the available ports on the AMC connector. The aggregate of all dot-spec fabric mappings we refer to here as the “port-map.”

The AMC specifications allow multiple options on how the ports on AMCs and AMC-based system can be used. The large number of options can improve the versatility of

the specification, but can also compromise interoperability. The intent of SCOPE is to provide guidance, via “Profiles,” which narrow the options and facilitates the creation of interoperable AMCs and AMC-based systems.

During the process of creating the Profiles, SCOPE could not find agreement on a common port-map based on the AMC specs as they stand today. Even with all of the versatility provided by the options, SCOPE still could not conclude on a mapping agreeable by all. The inability to reach a consensus view became a significant impediment to progress on both the AMC and MicroTCA Profiles. It became a stalemate in which SCOPE could not provide guidance which narrowed the options, because the options available could not be arranged in a manner that was suitable to common agreement.

Note that the issues weren’t so much with the AMC dot-specs themselves, taken individually. It was when combining the various dot-spec mappings into a system level mapping that the conflicts arose. Simultaneous usage of multiple fabrics, from multiple dot-specs, at the system-level and module-level, resulted in conflicts - particularly when exploring dual-star MicroTCA usage.

With the Profiles at a stalemate, SCOPE began exploring *if* a port-map that the members *could* align around could be created. Various options were considered, and eventually a conclusion was able to be reached. SCOPE determined the best course of action was to provide a Gap Analysis to PICMG, with recommendations and rationale on how to rectify the gaps.

The goal of the Gap Analysis is to have the gaps in the AMC specifications filled, such that SCOPE can profile its preference and guide the eco -system to interoperable AMCs and AMC -based systems.

The recommended port-mapping is meant to represent the mapping around which most AMCs and AMC-based systems can be built. Some application - and customer-specific mappings may fall outside the recommendations of this port-map, but that does not diminish the value of establishing the common base upon which the bulk of the eco -system can develop interoperable product.

The recommendations in this Gap Analysis were created based on the following primary considerations:

- If changes are needed, minimize disruption to current product
- Need for Dual-Star XAUI and Serial RapidIO capability in AMC -based systems (particularly MicroTCA for the Central Office)
- Re-use of AMCs between Simplex MicroTCA, Dual-Star (Central Office) MicroTCA, and AdvancedTCA

If the suppliers of AMCs and AMC -based systems follow the Profile guidelines, there can be significant interoperability benefits. Also, since the SCOPE Profiles will drive the market to a smaller number of implementation options, the volume of elements complying with the profile can increase, which in turn increases the ability of integrators to configure the interoperable elements into systems meeting a wide array of applications.

5. TERMS AND DEFINITIONS

AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunication Computing Architecture. Also known as AdvancedTCA™
CO	Central Office
Dot-spec	AMC.1, AMC.2, AMC.3, AMC.4
Dual-Star	A system-level fabric mapping where each FRU provides an independent fabric (or aggregate of fabrics) redundantly to independent redundant switching elements
MicroTCA	Micro Telecommunications Computing Architecture
Port-map	The aggregate of fabric mappings specified in the AMC dot-specs
Simplex	A system-level fabric mapping where each FRU provides one fabric (or a single aggregate of multiple fabrics) to a non-redundant singular switching element. Also known as Single-Star.

6. SUMMARY

6.1 Gaps in AMC Dot-Spec Port-Mapping

- 1) AMC.2 and AMC.4 could be inconsistently mapped, due to a recent change in AMC.2. Ensure AMC.2 and AMC.4 mappings are consistent.
- 2) XAUI/SRIO ports of AMC.2 and AMC.4 overlap the PCI-Express ports of AMC.1 on AMC ports 4-7.
- 3) The MicroTCA.0 specification's examples of dual-star fabric mapping (currently 4-7, 8-11) preclude the use of PCI-Express as an interconnect in a dual-star system given the current AMC dot-spec mappings, and would require updating to reflect any changes to the mapping.

6.2 Gaps indirectly related to Port-Mapping

- 1) MicroTCA.0: TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0.
- 2) AMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clock source (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH).

6.3 Recommendations

- 1) It is recommended that AMC.4 also provides the 1st SRIO port on 8-11, consistent with AMC.2.
- 2) It is recommended that AMC.2 and AMC.4 place the second XAUI/SRIO ports at Ports 20-17.
- 3) MicroTCA.0: It is recommended that ports 8-11 in the examples are mapped to the 'left' MCH, and ports 20-17 are mapped to the 'right' MCH, thereby allowing PCI-Express on 4-7 to be routed as a point-to-point topology.

4) It is recommended that MicroTCA.0 clarifies TCLKD usage and dual-star redundant-clock architecture for dual-star MicroTCA.

5) AMC.1: It is recommended that root-complex capable processor AMCs be capable of receiving *and providing* the PCI-Express Fabric Reference Clock to/from the FCLK signals. This will enable usage in point-to-point PCI-Express connections without a central Carrier/MCH-resident clock generator, *and* star/point-to-point connections where a central Carrier/MCH provides the clock.

7. DEEP-DIVE DETAIL OF CONSIDERATIONS

7.1 Common Options Region

Ports 0 & 1 are currently mapped with 1GbE. Ports 2 & 3 are mapped with SAS/SATA. No issues or conflicts were found with the mapping of the Common Options region.

7.2 PCI-Express

7.2.1 Background

PCI-Express finds substantial usage, as its name implies, as a peripheral component interconnect. In AdvancedTCA, PCI-Express is utilized to create 'classical' mezzanines where a Carrier-resident processor's functionality is expanded via peripheral PCI-Express based AMCs for I/O, co-processing, and other functional expansion. The PCI-Express link could be provided from the carrier-resident processor direct to the AMC, or it could be switched such that the carrier-resident root complex can control multiple peripheral modules.

Additionally, PCI-Express can be used as a peripheral interconnect for AMCs which themselves have a root-complex processor. PCI-Express could be routed to a switch such that one Processor AMC can control multiple peripherals, or it could be routed as a point-to-point interconnect between AMCs such that the processor has a dedicated slot for peripheral expansion.

PCI-Express is commonly provided in x1, x4, and x8 (x2 is uncommon, x16 is mainly for high-end PC video) configurations. Current PCI-Express is based on 2.5Gbaud (Gen1) signaling rates, with 5Gbaud (Gen2) coming in the near-term. SCOPE sees x4 Gen1 PCI-Express as a common usage today, and x4 Gen2 PCI-Express as a common usage as silicon becomes available.

It is acknowledged that Gen1 PCI-Express x8 is provided in some AMCs and AMC-based systems today as a means to provide additional bandwidth. But when looking to create a consistent port-map, the 8 ports end up occupying a significant partition of the system-level port-map, intruding on ports that could be better served by other uses. It is noted that PCI-Express Gen2 will enable double bandwidth via double-the-speed instead of double-the-ports. It is also noted that a x8 PCI-Express port can typically auto-negotiate down to a x4 link.

Given the satisfaction with x4 PCI-Express Gen1 today, the foreseen move to PCI-Express Gen2, and the difficulty with building a port-map around x8 PCI-Express, the port-map recommendations focus on enabling x4 PCI-Express as the most important usage.

7.2.2 PCI-Express (AMC.1) Mapping

The AMC.1 specification currently maps x4 PCI-Express to ports 4-7. With this established, there are no gaps in the AMC.1 specification in regards to port-mapping. However, other specifications 'collide' and utilize these ports 4-7 for other uses. This conflict is seen as a gap in the current specifications, and recommendations on how to rectify this collision will be provided in later sections.

As of 20th March 2007, a majority of SCOPE members expect that the most common usage of these ports 4-7 is expected to be x4 PCI-Express. In a system context, these ports can be applied in a point-to-point usage, or as a switched interconnect.

Note: See Section 7.7 for additional information on usage of the PCI-Express reference clock (AMC.0 FCLK).

7.3 Dual-Star XAUI/SRIO

7.3.1 Background

XAUI (10 Gigabit Ethernet) and x4 Serial RapidIO find usage as a data -plane and combined data/control-plane communication path within AdvancedTCA and MicroTCA systems. As bandwidth needs of communications infrastructure increases, and price points for these technologies come down over time, it is anticipated that usage will grow significantly.

As stated previously, PCI-Express is seen as a valuable peripheral interconnect. Even in systems which provide XAUI/SRIO as a data/control-plane path, PCI-Express is still useful for aggregating processing, co-processing, and I/O functions.

7.3.2 XAUI (AMC.2) / SRIO (AMC.4) Mapping

The current AMC.2 specification places the first XAUI link at ports 8-11, and the second link at ports 4-7. This was a recent shift. Previously the links were reversed. The current AMC.4 specifications place the first SRIO link at ports 4-7, and the second at 8 -11 (opposite latest AMC.2).

The AMC.2 mapping was recently changed to accommodate the consistent usage of PCI-Express on ports 4-7. The first XAUI port was moved to ports 8 -11 to enable co-existent heterogeneous usage of a single XAUI and x4 PCI-Express within an AMC and AMC-based systems. SCOPE agrees with this change to AMC.2, but wants to ensure that AMC.4 also follows suit so that the overall Port-Map is consistent.

Gap: AMC.2 and AMC.4 could be inconsistently mapped, due to a recent change in AMC.2. Ensure AMC.2 and AMC.4 mappings are consistent.

It is recommended that AMC.4 also provides the 1st SRIO port on 8-11, consistent with AMC.2.

Resolving this Gap solves the system-level conflict of the port-map between PCI-Express with single XAUI *and* SRIO links.

7.3.3 PCI-Express with Dual-Star XAUI/SRIO

However, a conflict remains for AMCs providing dual-XAUI/SRIO ports and wishing to leverage PCI-Express as an interconnect. The second XAUI/SRIO port will still overlap PCI-Express on 4-7.

A majority of SCOPE members see an important need for a port map that supports a single class of AMCs that:

- Simultaneously operates x4 PCI-Express and redundant 10GbE fabric interfaces, mainly for MicroTCA applications, and
- Simultaneously operates x4 PCI-Express and 10GbE fabric interfaces, mainly for ATCA applications.

Hence, there is a need for orthogonal mapping of x4 PCI-Express and redundant 10GbE ports in the AMC fabric interface, to enable one module which supports both usages.

It is important for the eco-system to understand SCOPE's desire to enable AMCs and MicroTCA for Central Office telecom applications. Of particular note is the capability to provide redundant switch-fabrics to each FRU, with redundant switching elements (i.e. MicroTCA MCH) such that there is no single point-of-failure on the fabric.

It is also important to restate the continued need for PCI-Express capability, even for dual-star fabric systems. In large form-factors such as AdvancedTCA, it is possible and desirable to fit all functionality into one blade. With all functions in-blade on ATCA, there is no need for a peripheral interconnect between ATCA blades, and systems can be constructed with the simple 1GbE Base Channel and 10GbE XAUI as a data-plane Fabric Channel.

However, with the small form-factor of AMC, it is noted that some functions may not be able to completely fit onto a single blade. Thus, functions can be divided into pairs of blades, with PCI-Express as board-to-board interconnect between them. This is where PCI-Express remains desirable as a peripheral interconnect, even in Dual-star XAUI/SRIO systems.

Gap: XAUI/SRIO ports of AMC.2 and AMC.4 overlap the x4 PCI-Express ports of AMC.1 on AMC Ports 4-7.

Due to the value of PCI-Express and the need for dual-star XAUI/SRIO capable AMCs and AMC-based systems, it is recommended that AMC.4 and AMC.2 find a new location other than Ports 4-7 for their second XAUI and x4 SRIO ports.

7.3.4 Resolving the PCI-Express with Dual-Star XAUI/SRIO Gap

This begs the question: "So where do we put the 2nd XAUI/SRIO ports?" Rather than simply note the gap and leave it at that, SCOPE has investigated potential options, and has a suggestion.

Ports 0-3 have been found acceptable for 1GbE and storage connectivity. Ports 4-7 are utilized by PCI-Express. Ports 8-11 are utilized by the 1st XAUI/SRIO and up to 4 GbE ports. That leaves either 12-15, or 20-17 as the remaining places the 2nd XAUI/SRIO ports can fit within the port-map.

Note here that the nomenclature “12-15” and “20-17” is used in this document. The flipped-numbering nomenclature for 20-17 is a consequence of the AMC.0 specification calling for port-usage of the extended-options region to start from Port 20 and count down for those four ports. Numbering the ports 12-15 is a consequence of the usage of Port 12 as an Update Channel usage, and so we start at 12 and count up for those four ports.

Note that Port 16 was recently re-provisioned as extra telecom clocks in AMC.0 R2.0 and is no longer considered available in the Port-Map.

For Ports 12-15, Port 12 is often used in current systems as an inter-AMC Update Channel across two Carriers. This is particularly useful for communication for Automatic Protection Switching (APS) for SONET/SDH optical AMCs.

Otherwise, Ports 12-15 and 20-17 are used for RTM I/O from AMCs to their ATCA Carrier RTMs. If Port 12 is seen as a typical or reserved location for inter-AMC Update Channels, then Ports 20-17 may be a better location.

By placing the 2nd XAUI/SRIO ports on 20-17, we overlap ports typically used by AMCs for RTM I/O. Note that Dual-Star capable AMCs will typically be destined for MicroTCA which currently does not accommodate transition-modules. And AMCs designed with a lot of ports for RTM I/O will typically find those ports unused in MicroTCA for the Central Office – which will instead use the front-access front-panel ports of the AMC. So it appears the conflict is minimal.

However, it is noted that there may be some potential synergistic uses for an AMC providing their second XAUI or SRIO on 20-17, and having that AMC cross-over for usage in AdvancedTCA. As 20-17 are typically routed for RTM I/O, vendors could leverage this and provide this second XAUI/SRIO as just another rear I/O port available to the RTM.

Due to the usage of Port 12 as an inter-AMC Update Channel, and potential synergy of 2nd XAUI/SRIO overlapping RTM I/O ports, it is recommended that AMC.2 and AMC.4 place the second XAUI/SRIO ports at Ports 20-17.

7.4 RTM I/O

AMCs can utilize Extended Options Region Ports 20-12 as RTM I/O ports, per AMC.0. For AMCs not providing dual-star XAUI/SRIO Fabric support, this continues to remain true. For AMCs providing dual-star XAUI/SRIO Fabric support, the second XAUI/SRIO port could also be utilized as a XAUI/SRIO interconnect to RTM I/O in ATCA Carriers, consistent with current usage.

7.5 Inter-AMC Point-to-Point Connectivity

Port 12 is often used in current systems as an inter-AMC communications path. It can be used between two AMCs within the Carrier, or mapped to one of the five ports in the Update Channel defined in PICMG 3.0 for communications across two AdvancedTCA Carriers. This is particularly useful for Automatic Protection Switching (APS) for SONET/SDH optical AMCs, but could prove useful in other applications in the future. Thus, SCOPE avoids conflicting with this usage in the recommendations.

It is noted that all of 12-15 could potentially be used as Inter-AMC Point-to-Point connectivity for MicroTCA. But it is also noted that restrictions on the number of ports in the Update Channel provided by PICMG 3.0 could limit the usefulness of wider connectivity in AdvancedTCA (there are 5 ports in the ATCA Update Channel – most logically one [Port 12] per AMC in a 4x AMC configuration, plus one for the Carrier itself).

It is also noted that AMCs that need to provide a x8 PCI-Express port could put the second 4 ports on 12-15; but this is outside of the most important usages and not considered a gap. We leave it to the AMC.1 specification to decide whether it's better to split x8 PCI-Express across 4-7 and 12-15, or leave it as it is at 4-11.

7.6 Telecom Clocks

AMC.0 R2.0 recently provisioned Port 16 for Telecom Clocks TCLKC and TCLKD. TCLKC was provisioned to provide the third telecom clock without overlap with the fabric reference clock of PCI-Express, which is now FCLK. As there are two differential pairs to a port, the second pair was reserved as TCLKD.

The definition of Telecom Clocks as defined in AMC.0 is a welcome update, to the extent that the clocks are defined. However, it is noted that TCLKD, and clock mapping for MicroTCA dual-star and redundant-clock architectures, is not well defined. It is the understanding of SCOPE that this usage was consciously 'deferred' by AMC.0 such that MicroTCA.0 could come in later and settle the details on how this clock could be used in dual-star MicroTCA systems.

Gap: TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0.

It is recommended that MicroTCA.0 take the lead in clarifying TCLKD usage and dual-star redundant-clock architecture for dual-star MicroTCA. Whether AMC.0 would need "re-updated" based on that clarification would depend on the content incorporated into MicroTCA.0.

7.7 Fabric Reference Clock

In developing this Port-map, it was noted that for a Dual-Star MicroTCA system which provides PCI-Express between AMC pairs, that if the PCI-Express Fabric Clock is provided by the MCH, this is a single-point-of-failure. This may be unacceptable. Given that the dual-star (high-availability) usage may use point-to-point PCI-Express between module pairs, it seems logical that the root-complex AMC could be able to provide the clock directly to its peripheral pair in this usage case. As these AMCs would be paired, just the two PCIe-mated boards would be the point of failure, and not the whole system.

Gap: AMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clocksource (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH).

It is recommended that AMC.1 provide more explicit guidance on who provides the PCI-Express Fabric Reference Clock. Generally the Reference Clock will be provided by the ATCA Carrier or PCI-Express capable MCH on the AMC FCLK signals. However, this can be a single-point of failure or simply not provided in systems with point-to-point PCI-Express connectivity and without PCI-Express switching provided by the MCH.

It is recommended that root-complex capable processor AMCs be capable of receiving *and providing* the PCI-Express Fabric Reference Clock to/from the FCLK signals. This will enable usage in point-to-point PCI-Express connections without a central Carrier/MCH-resident clock generator, *and* star/point-to-point connections where a central Carrier/MCH provides the clock.

In systems requiring high-availability, but only having PCIe connectivity point-to-point, it would be desirable that each root-complex AMC provides the clock to its peripheral AMC. Currently, the Carrier (the MCH in MicroTCA) can be a single -point-of-failure if it is the sole provider of the PCI-Express clock. This may be acceptable in many cases, but not in the case of dual-star MicroTCA with PCI-Express solely provided as an inter-AMC point-to-point interconnect.

7.8 MicroTCA

The MicroTCA.0 specification currently provides some examples of backplane mappings, with ports 4-7 provided to the 'left' MCH and 8-11 to the 'right' MCH.

Gap: MicroTCA.0: The MicroTCA.0 specification's examples of dual-star fabric mapping (currently 4-7, 8-11) preclude the use of PCI-Express as an interconnect in a dual-star system given the current AMC dot-spec mappings, and would require updating to reflect any changes to the mapping.

It is recommended that ports 8-11 in the examples are mapped to the 'left' MCH, and ports 20-17 are mapped to the 'right' MCH, thereby allowing PCI-Express on 4-7 to be routed as a point-to-point topology.

8. AMC PORT-MAP RECOMMENDATION

Port No	AMC Port area	Port use
TCLKA	Telecom Clocks*	Telecom clock (to AMC)
TCLKB		Telecom clock (from AMC)
TCLKC		Telecom clock (to AMC)
TCLKD		Telecom clock (from AMC)
FCLK	Fabric Reference Clock	PCI-Ex 100MHz
0	Common options region	1GbE_1
1		1GbE_2
2		SAS/SATA_1
3		SAS/SATA_2
4	Fat pipes region	Point-to-Point 1 Port 1 (PCle_1)
5		Point-to-Point 1 Port 2 (PCle_2)
6		Point-to-Point 1 Port 3 (PCle_3)
7		Point-to-Point 1 Port 4 (PCle_4)
8		Fabric 1 Port 1 (1GbE_3 / 1 st XAUI/SRIO_1)
9		Fabric 1 Port 2 (1GbE_4 / 1 st XAUI/SRIO_2)
10		Fabric 1 Port 3 (1GbE_5 / 1 st XAUI/SRIO_3)
11		Fabric 1 Port 4 (1GbE_6 / 1 st XAUI/SRIO_4)
12	Extended options region	Point-to-Point 2 Port 1 (AMGAMC Point-to-Point_1 / Update channel_1 / RTM I/O_8)
13		Point-to-Point 2 Port 2 (AMGAMC Point-to-Point_2 / RTM I/O_7)
14		Point-to-Point 2 Port 3 (AMGAMC Point-to-Point_3 / RTM I/O_6)
15		Point-to-Point 2 Port 4 (AMGAMC Point-to-Point_4 / RTM I/O_5)
17		Fabric 2/RTM Port 4 (2nd XAUI/SRIO_4 / RTM I/O_4)
18		Fabric 2/RTM Port 3 (2nd XAUI/SRIO_3 / RTM I/O_3)
19		Fabric 2/RTM Port 2 (2nd XAUI/SRIO_2 / RTM I/O_2)
20		Fabric 2/RTM Port 1 (2nd XAUI/SRIO_1 / RTM I/O_1)

Legend

	MicroTCA: To/From MCH 1
	MicroTCA: To/From MCH 2

Notes on Clocks:

* TCLK usage/mapping for dual-redundant MicroTCA clock architecture needs updated/defined, now that AMC.0 R2.0 has an additional TCLKD.

** For Carriers & MicroTCA MCHs, it is recommended that all four TCLKs should be bi-directional capable, to accept Master Clock Generator [MCG] or Line-Card AMCs.