

# AdvancedMC™ Hardware Profile

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Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

SCOPE Alliance  
c/o IEEE-ISTO  
445 Hoes Lane  
Piscataway, NJ 08854  
Attn: Board Chairman

or

For questions or feedback, use the Web forms found under the Contacts tab on the SCOPE Alliance Web site at <http://www.scope-alliance.org>

## **1. PURPOSE**

The purpose of this document is to provide guidelines to standardization bodies, vendors and end users that want to migrate from proprietary solutions to the open standards based platform AdvancedMC™. The AdvancedMC specification of the PCI Industrial Computer Manufacturers Group (PICMG) covers many hardware aspects of modular, scalable platforms for telecommunications networks and other uses. The document will also help the adopters of AdvancedMC™ specifications by identifying the features important for the telecom equipment providers.

This document provides guidelines, narrows options and prioritizes requirements, with the intention of facilitating the creation of fully compliant, interoperable AdvancedMC. It also identifies gaps which, if resolved, should facilitate better operational utility and interoperability of AdvancedMC between MicroTCA and AdvancedTCA™ systems as well as proprietary systems utilizing AdvancedMC as components. This profile was prepared by members of the SCOPE Alliance AdvancedMC Working Group, after consolidating their views on what properties of MicroTCA and AdvancedTCA systems is important.

Although AdvancedMC has many potential markets, including industrial, scientific, medical, military and more, this profile focuses on the use of AdvancedMC in telecommunications networks. Furthermore, although AdvancedMC is applicable to central office applications, as well as to outside plant and customer premises applications, this profile is focused on central office applications of AdvancedMC as a first step.

The contents of this AdvancedMC profile are subject to change as the application requirements mature, and as the standards are revised. The SCOPE Alliance will revise and reissue the AdvancedMC profile, if necessary, in response to such changes.

This AdvancedMC profile document is not a substitute for the AdvancedMC specifications that are maintained by, and can be obtained from, PICMG.

In essence, the main purpose of this document is to create a solid competitive environment for common building blocks and to avoid a fragmented market.

## 2. AUDIENCE

The AdvancedMC profile document is intended for the following targeted audiences:

- Hardware vendors
- Manufacturers of AdvancedMC, AdvancedTCA blades and shelf building blocks, and also base platform integrators
- Telecom equipment manufacturers who are building or planning to build systems based on AdvancedMC specifications
- Standardization bodies and related trade associations, to make them aware of gaps in AdvancedMC specifications definitions and to offer them proposals or requirements for needed and necessary amendments.

## 3. REFERENCES

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## **INTRODUCTION**

The PCI Industrial Computer Manufacturers Group (PICMG) has defined an open, standard platform for telecom equipment called AdvancedMC™ [3]. The AdvancedMC specification defines an architecture for modular components that can be quickly integrated to deploy high performance, carrier grade service solutions. In essence, the components from different vendors will inter-operate with each other and, thus, giving flexibility to combine components from different vendors. The AdvancedMC specification also consists of a number of sub-specifications, so-called DOT specifications [4] ~ [7], handling a number differencing alternatives, mainly choice of switch fabric. The AdvancedMC profile document has not treated this dot specification separated, instead as a part of the AdvancedMC profile document.

The SCOPE Alliance has identified parts of the AdvancedMC specification that allow multiple implementation options, and has narrowed down the choices to a smaller subset that, in its view, serve the needs of central office applications. The SCOPE Alliance has also identified gaps in AdvancedMC and related specifications, i.e., deficiencies in the specification that should be closed to avoid implementation and interoperability problems. This AdvancedMC profile document addresses these issues and gaps.

In addition the document also discusses some properties of complete systems such as MicroTCA™ [1] and AdvancedMC™ [2], detailed descriptions of the feature set could be found in the PICMG specifications and the corresponding SCOPE Alliance documents for an AdvancedTCA Hardware Profile [9] and a MicroTCA Profile [10]. Also in addition is the SCOPE Alliance document AdvancedMC Port Map Gap Analysis [11] giving guidelines of efficient use of ports in a mixed fabric environment.

The AdvancedMC specification covers many aspects of design and operation including mechanical and electrical characteristics, data transport, and more. While specifications of many features are comprehensive, some aspects are left ambiguous to allow customization and future extensions. As a result the specification has become unwieldy and demanding for vendors to formally claim compliance. Consequently, the vendors are uncertain of development effort in making a marketable platform product.

This AdvancedMC profile document identifies a subset of features from the AdvancedMC specification that are sufficient to address most of service & control as well as data of the telecom market's needs. The equipment vendors can use this as reference to develop their products in phases and yet generate revenue with AdvancedMC formally.

This AdvancedMC profile document is the result of an effort to protect long-term investments of the customers. It is consolidation of features that are required from a platform to support most of the current and future telecommunication applications within the central office.

## 4. TERMS AND DEFINITIONS

<b>AdvancedMC</b>	Advanced Mezzanine Card
<b>AdvancedTCA</b>	Advanced Telecommunication Computing Architecture. A registered trademark of PCI Industrial Computer Manufacturers Group® referring to PICMG3.x set of standards.
<b>AMC</b>	When the “AMC” is used on its own, it can refer to the AMC .0 specifications or it can generically refer to the family of AMC specifications, depending on the context.
<b>APS</b>	Automatic Protection Switching. The capability of a system to switch from a failed interconnect signal to a redundant signal.
<b>Backplane</b>	A passive circuit blade providing connectivity of front blade Slots in the shelf. The connection includes high-speed differential pairs, power distribution, management, and auxiliary signal connections.
<b>BIOS</b>	Basic Input/Output System. The firmware code run by a computer when it is first powered on.
<b>CPU</b>	Central Processing Unit. The central processing functional element of a computer.
<b>CO</b>	Central Office.
<b>CPE</b>	Customer Premises Equipment.
<b>Dual Star Topology</b>	An interconnect fabric topology in which two switch resources provide redundant connections to all end points within the network. A pair of switch boards provides redundant interconnects between node blades.
<b>EMC</b>	Electro Magnetic Compatibility.
<b>ETSI</b>	European Telecommunications Standards Institute. An independent, non-profit, standards organization of the telecommunications industry (equipment makers and network operators) in Europe.
<b>FCLCK</b>	Fabric Clock A. A signal used in AdvancedMC to synchronize PCI Express communication links.
<b>Face Plate</b>	The front-most element of a Module, attached perpendicular to the PCB, and serves to mount connectors, indicators, controls, and also seals the front of the Subrack for airflow and EMC.
<b>FRU</b>	Field Replaceable Unit. Any entity that can be replaced by a user in the field
<b>FUMI</b>	Firmware Upgrade Management Instrument. A management instrument defined by SA Forum SAI-HPI-B.02.01 [12] for remote firmware upgrades.
<b>GbE</b>	Gigabit Ethernet
<b>HDD</b>	Hard Disk Drive. A non-volatile storage device that stores digitally encoded data on rapidly rotating platters with magnetic surfaces.
<b>HPI</b>	Hardware Platform Interface defined by the SA Forum. A standard interface between the hardware platform management system and the middleware or other application software.
<b>HPM.1</b>	Hardware Platform Management [8]. A PICMG specification covering the upgrade capability of the firmware of IPM controllers of modular platforms.
<b>JTAG</b>	Joint Test Action Group. A standard for serial testing of electronic modules.
<b>LED</b>	Light Emitting Diode. A semiconductor device that emits incoherent narrow-spectrum light when electrically biased in the forward direction of the p-n junction.
<b>µTCA or MicroTCA</b>	Micro Telecommunications Computing Architecture. A PICMG specification in which AdvancedMC modules plug directly into a backplane.

<b>MTBF</b>	Mean Time Between Failures.
<b>MTTR</b>	Mean Time To Repair.
<b>NEP</b>	Network Equipment Provider
<b>PCI-E</b>	PCI Express. A computer interface standard common in PCs.
<b>PICMG</b>	PCI Industrial Computer Manufacturers Group®
<b>POST</b>	The Power-on Self test is a diagnostic testing sequence run by the CPU's BIOS as the computer's power is initially turned on. After performing the POST the BIOS loads and starts the master boot from disk or another storage device.
<b>RAID</b>	Redundant Array of Inexpensive Disks.
<b>ROHS</b>	Reduction of Hazardous Substances. A standard for the elimination of six hazardous materials from electronics.
<b>RTM</b>	Rear Transition Module. An 8U x 70 mm x 6 HP assembly installed into the rear portion of a Shelf and mated with a front blade through Zone 3 connectors to provide I/O connectivity.
<b>SA Forum</b>	Service Availability™ Forum. A consortium of communications and computing companies that develop and publish high availability and management software interface specifications.
<b>SAS/SATA</b>	Serial Attached SCSI / Serial Advanced Technology Attachment. Standard interfaces to disk drives.
<b>SCSI</b>	Small Computer System Interface. A set of standards for physically connecting and transferring data between computers and peripheral devices.
<b>Shelf</b>	The Shelf consists of the subrack, backplane, boards, cooling devices, RTMs, power supplies, etc.
<b>SRIO</b>	Serial Rapid I/O.
<b>TCLK or TCLKA TCLKB TCLKC TCLKD</b>	Telecommunications CLocks, A, B, C and D. A set of signals on the AdvancedMC to synchronize telecommunications I/O signals.
<b>TEM</b>	Telecommunication Equipment Manufacturer
<b>U</b>	Unit of vertical height defined in IEC 60297-1 rack, shelf, and subrack height increments. 1U = 44.45 mm = 1.75 inches.
<b>WEEE</b>	Waste Electrical and Electronic Equipment. A directive to improve the recycling of electronic equipment.
<b>XAUI</b>	X (i.e. 10) Attachment Unit Interface. A physical layer that carries a 10 Gb Ethernet on four serial lanes.

## **5. RECOMENDASIONS**

The AdvancedMC™ specification describes extensive sets of features and options. The SCOPE Alliance AdvancedMC Working Group has developed a profile of the AdvancedMC specification, and has identified certain gaps in the AdvancedMC specification. The AdvancedMC Profile is shown below in tabular form grouped into the following nine categories:

1. General
2. Mechanical
3. Hardware Management
4. Power
5. Thermal
6. Interconnect
7. Regulatory
8. Availability
9. Other

The gaps shown in the AdvancedMC Profile Table identify features that the SCOPE Alliance AdvancedMC Working Group regards as requirements that should be added to the AdvancedMC specification. The gaps are prioritized as High, Medium and Low, which are defined as follows:

- High - Start implementation now.
- Medium - Start implementation as soon as possible.
- Low - Start implementation as soon as the gaps prioritized as High and Medium have been implemented.

The priorities of the gaps give advice to the community on the relative importance of the gaps and the order in which to implement them, as the SCOPE Alliance AdvancedMC Working Group sees it.

**AdvancedMC Profile Table**

The AdvancedMC Profile Table provides a consolidated view of the needs of network equipment providers for control and service plane applications in the central office environment based on AdvancedMC. The gaps identified in the AdvancedMC specifications, along with their priorities, are marked starting with “**Gap (High/Medium/Low Priority)**” and are highlighted in bold.

<b>SCOPE Alliance AdvancedMC Profile Requirements</b>			
<b>ID</b>	<b>Requirement group</b>	<b>SCOPE Alliance Consensus View</b>	<b>Comment</b>
<b>1. GENERAL</b>			
1.1	<b>Philosophy/use scope</b>	Leverage synergies between AdvancedTCA, MicroTCA and proprietary/customized system for central office equipment. Modular platform for multiple applications.	Three segments: 1) CO – NEBS 3 compliant/ETSI including back office equipment. 2) Outdoor. 3) CPE – Enterprise.  This profile will focus on segment 1.
1.2	<b>Simplex/duplex interfaces (single/dual stars)</b>	Duplex interfaces: GbE, SAS/SATA, XAUI/SRIO and Clocks. Simplex interfaces seen as a subset of duplex interfaces.  Simplex interfaces: PCI Express and APS	The AdvancedMC interfaces are simplex, as kind, but duplicated giving a duplex functionality.
1.3	<b>Interoperability</b>	AdvancedMC interoperability must be guaranteed for full compliance to AMC.0 R2.0 specifications.  AdvancedMC requirements in this profile shall apply (without conflict) both for AdvancedTCA and MicroTCA form factors.	
<b>2: MECHANICAL</b>			
2.1	<b>Corporate Appearance</b>	If there is only one common approach / methodology, NEPs will use it as long as all requirements are met (e.g., EMC, easy handling, etc.). If there is no common approach, there must be supplier independent interchangeability of faceplates and handles.  The company trademark should be put on a label on the front board (real estate on the blade front plate is needed).  At least the following AMC.0 defined LEDs must be supported on each Advanced Mezzanine	<b>Gap (Medium Priority): PICMG should rigorously specify a “blank canvas” for attributes associated with faceplates, etc. The specification should include EMC sealing interface, faceplate and ejector handle mounting and operation, common LED locations, and labeling areas.</b>  <b>If there is no common approach, a supplier independent interchangeability of faceplates and handles is required. For this PICMG should rigorously specify; EMC sealing interface, faceplate and ejector handle mounting and operation, common LED locations,</b>

		<p>Card: Hot swap (blue LED), LED1 (Out Of Service) and LED2 (health).</p> <p>It should be possible to mount NEP-specific front plate assemblies. As handles and handle switches are not specified by the standard, they might as well be a part of the corporate appearance.</p> <p>Most NEPs require a custom label and the ability to modify FRU data.</p> <p>It should also be possible to re-label (replacement of) label stickers.</p> <p>Look &amp; Feel sticker, plus ability to modify FRU data, is required.</p>	<b>and labeling areas to make full interoperability possible.</b>
<b>2.2</b>	<b>Form factors of AdvancedMC modules</b>	<p>ATCA: midsize single width preferred for conventional carriers, full-size single width preferred for cut-away carriers.</p> <p>MicroTCA: Compact and full-size single width preferred.</p>	Compact and midsize modules could be converted by change of faceplate or by adding a 2 respective 3 HP filler panels or other mechanical solutions. Thermal requirement of the target slot /bay must then be met.
<b>2.3</b>	<b>AdvancedMC Faceplate</b>	AdvancedMC faceplate is expected to be compliant with release R2.0 of the AdvancedMC specification.	<p>Custom and company dependant.</p> <p>Standard AdvancedMC with customer appearance adapted faceplate.</p>

### 3. HARDWARE MANAGEMENT

<b>3.1</b>	<b>Upgrade</b>	Support for MMC update via SA Forum HPI FUMI, detailed in SAI-HPI-B.02.01, is required, HPM.1 preferred.	Remote firmware upgrade to enable automatic procedure for firmware upgrade without service interruption with fallback feature.
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### 4. POWER

<b>4.1</b>	<b>Power budget</b>	<p>Power dissipation as per recommendation in the AdvancedMC specification.</p> <p>Power feed 80W as per AdvancedMC specification.</p>	<p>However, the SCOPE Alliance is not convinced that this is the right level, these are the best figures we could state as per today.</p> <p>Maximum power dissipation is a vendor competitive edge factor.</p> <p>Power feed could be much larger than the power dissipation (e.g. power over Ethernet application)</p>
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5. THERMAL			
5.1	<b>AdvancedMC thermal requirement</b>	<p>Hydraulic impedance must be specified by the board supplier as per AMC.0 R2.</p> <p>Air flow over pressure drop curve (speed steps, failure cases) for AdvancedMC must be specified by the board supplier as per AMC.0 R2.</p> <p>Maximum operation inlet air temperature versus airflow curve must be specified by the board supplier.</p> <p>The AdvancedMC supplier shall specify the supported operating ambient air temperature range for both short term and long term conditions (in accordance with NEBS requirements) for information on short term time limits as per AMC.0 R2 specification but the AdvancedMC supplier shall also state if the board can cope or not with 65°C inlet air temperature for short terms and 52°C for long terms for Single AdvancedMC (in accordance with NEBS requirements), 62°C and 48°C for Double AdvancedMC.</p> <p>The AdvancedMC supplier must state if the board maximum output temperature is 70°C or more.</p>	<p><b>Gap (Medium Priority): Specification on high operation temperature range is missing:</b></p> <p><b>Method to be defined in PICMG, for better specification, prediction and management of thermals, e.g. definition of minimum/maximum air impedance, inlet air temperature, inlet air temperature when stacking etc.</b></p>
5.2	<b>Air flow path</b>	Bottom to top.	Bottom is to be considered to be the ejector handle edge of the AdvancedMC.
5.3	<b>Operating temperature</b>	<p>As per AdvancedMC specification.</p> <p>Normal operating temperature range: +5°C to +40°C ambient air.</p> <p>Short term (96 hours max): -5°C to 55°C.</p> <p>Should follow NEBS temperature criteria for storage and transportation.</p>	<p>ETSI Class 3.1E GR-63</p> <p>Cold start required only in normal operating conditions.</p>

**6. INTERCONNECT**

<p><b>6.1</b></p>	<p><b>AdvancedMC Port Mapping</b></p>	<p>High-speed serial lane and clock port mapping should follow the SCOPE Alliance Port Mapping recommendations, published May 2007.</p> <p>The PICMG AMC.0 specification provides a framework definition for fabric port interconnect usage provided by AdvancedMC modules. Subsidiary specifications (referred to as "dot specifications" e.g. AMC.1, AMC.2, etc.) were created to define the usage of ports for interconnects such as PCI-Express, Ethernet, SAS/SATA, and Serial RapidIO. Each of these dot-specs maps a particular fabric-type into the available ports on the AdvancedMC connector. The aggregate of all dot-specifications fabric mappings we refer to here as the "port-map."</p> <p>The AdvancedMC specifications allow multiple options on how the ports on AdvancedMC and AdvancedMC-based system can be used. The large number of options can improve the versatility of the specification, but can also compromise interoperability. The intent of SCOPE is to provide guidance, via "Profiles," which narrow the options and facilitates the creation of interoperable AdvancedMC and AdvancedMC-based systems.</p> <p>During the process of creating the Profiles, SCOPE could not find agreement on a common port-map based on the AdvancedMC specs as they stand today. Even with all of the versatility provided by the options, SCOPE still could not conclude on a mapping agreeable by all. The inability to reach a consensus view became a significant impediment to progress on both the AdvancedMC and MicroTCA Profiles. It became a stalemate in which SCOPE could not provide guidance which narrowed the options, because the options available could not be arranged in a manner that was</p>	<p><b>Gap (High Priority):</b> Current state of AdvancedMC and MicroTCA specifications, as well as current AdvancedMC and MicroTCA backplane and MCH designs, do not necessarily follow the SCOPE Alliance Port Mapping recommendations. These different views must converge. Recommended port map in accordance with the SCOPE port map gap-analysis.</p> <p><b>Gap (High Priority):</b> AMC.2 and AMC.4 could be inconsistently mapped, due to a recent change in AMC.2. Ensure AMC.2 and AMC.4 mappings are consistent. It is recommended that AMC.4 also provides the 1<sup>st</sup> SRIO port on 8-11, consistent with AMC.2.</p> <p><b>Gap (High Priority):</b> XAUI/SRIO ports of AMC.2 and AMC.4 overlap the x4 PCI-Express ports of AMC.1 on AdvancedMC Ports 4-7. Due to the value of PCI-Express and the need for dual-star XAUI/SRIO capable AdvancedMC and AdvancedMC-based systems, it is recommended that AMC.4 and AMC.2 find a new location other than Ports 4-7 for their second XAUI and x4 SRIO ports.</p> <p><b>Gap (High Priority):</b> TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0. It is recommended that MicroTCA.0 take the lead in clarifying TCLKD usage and dual-star redundant-clock architecture for dual-star MicroTCA. Whether AMC.0 would need "re-updated" based on that clarification would depend on the content incorporated into MicroTCA.0.</p> <p><b>Gap (High Priority):</b> AMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clock source (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH). It is recommended that AMC.1 provide more explicit guidance on who provides the PCI-Express Fabric</p>
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		<p>suitable to common agreement.</p> <p><b>Recommended SCOPE port map:</b></p> <p><b>Telecom Clocks, see Table 1:</b>  TCLKA: Telecom clock A  (to AdvancedMC)  TCLKB: Telecom clock B  (from AdvancedMC)  TCLKC: Telecom clock C  (to AdvancedMC)  TCLKD: Telecom clock D  (from AdvancedMC)</p> <p><b>Fabric Reference Clock:</b>  FCLK: PCI-E 100MHz  (to/from AdvancedMC)</p> <p>Notes on Clocks:  * TCLK usage/mapping for dual-redundant MicroTCA clock architecture needs updated/defined, now that AdvancedMC.0 R2.0 has an additional TCLKD.  ** For Carriers &amp; MicroTCA MCH's, it is recommended that all four TCLKs should be bi-directional capable, to accept Master Clock Generator [MCG] or Line-Card AdvancedMCs.</p> <p><b>Common options region:</b>  Port 0: 1GbE_1  Port 1: 1GbE_2  Port 2: SAS/SATA_1  Port 3: SAS/SATA_2</p> <p><b>Fat pipes region:</b>  Port 4: Point-to-Point 1 Port 1  (PCle_1)  Port 5: Point-to-Point 1 Port 2  (PCle_2)  Port 6: Point-to-Point 1 Port 3  (PCle_3)  Port 7: Point-to-Point 1 Port 4  (PCle_4)  Port 8: Fabric 1 Port 1  (1GbE_3 / 1<sup>st</sup>  XAUI/SRIO_1)  Port 9: Fabric 1 Port 2  (1GbE_4 / 1<sup>st</sup>  XAUI/SRIO_2)  Port 10: Fabric 1 Port 3  (1GbE_5 / 1<sup>st</sup>  XAUI/SRIO_3)  Port 11: Fabric 1 Port 4  (1GbE_6 / 1<sup>st</sup></p>	<p><b>Reference Clock.</b> Generally the Reference Clock will be provided by the ATCA Carrier or PCI-Express capable MCH on the AdvancedMC FCLK signals. However, this can be a single-point of failure or simply not provided in systems with point-to-point PCI-Express connectivity and without PCI-Express switching provided by the MCH.</p> <p>It is recommended that root-complex capable processor AdvancedMCs be capable of receiving <i>and providing</i> the PCI-Express Fabric Reference Clock to/from the FCLK signals. This will enable usage in point-to-point PCI-Express connections without a central Carrier/MCH-resident clock generator, <i>and star/point-to-point connections</i> where a central Carrier/MCH provides the clock.</p> <p>In systems requiring high-availability, but only having PCI-Express connectivity point-to-point, it would be desirable that each root-complex AdvancedMC provides the clock to its peripheral AdvancedMC. Currently, the Carrier (the MCH in MicroTCA) can be a single-point-of-failure if it is the sole provider of the PCI-Express clock. This may be acceptable in many cases, but not in the case of dual-star MicroTCA with PCI-Express solely provided as an inter-AdvancedMC point-to-point interconnect.</p>
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		<p>XAUI/SRIO_4)</p> <p><b>Extended options region:</b>  Port 12: Point-to-Point 2 Port 1  (AdvancedMC-AdvancedMC Point-to-Point_1 / Update channel_1 / RTM I/O_8)  Port 13: Point-to-Point 2 Port 2  (AdvancedMC-AdvancedMC Point-to-Point_2 / RTM I/O_7)  Port 14: Point-to-Point 2 Port 3  (AdvancedMC-AdvancedMC Point-to-Point_3 / RTM I/O_6)  Port 15: Point-to-Point 2 Port 4  (AdvancedMC-AdvancedMC Point-to-Point_4 / RTM I/O_5)  Port 16: Defined as TCLOCK  Port 17: Fabric 2/RTM Port 4  (2nd XAUI/SRIO_4 / RTM I/O_4)  Port 18: Fabric 2/RTM Port 3  (2nd XAUI/SRIO_3 / RTM I/O_3)  Port 19: Fabric 2/RTM Port 2  (2nd XAUI/SRIO_2 / RTM I/O_2)  Port 20: Fabric 2/RTM Port 1  (2nd XAUI/SRIO_1 / RTM I/O_1)</p>	
6.2	<b>AdvancedMC base interface</b>	1 GE dual star (PICMG® AMC.2, Type E2)	Port 0 and port 1
6.3	<b>AdvancedMC fabric interface</b>	<p>Fabric is Ethernet or sRIO technology 10 Gbits per slot, dual star. (PICMG® AMC.2, Type 6* or PICMG® AMC.4, Type 8*)</p> <p>PCI-Express 4x is seen as a valuable peripheral interconnect. Even in systems which provide XAUI/SRIO as a data/control-plane path, PCI-Express is still useful for aggregating processing, co-processing, and I/O functions. (PICMG® AMC.1, Type 4)</p>	<p>* Recommended port map in accordance with the SCOPE port map gap-analysis:</p> <ul style="list-style-type: none"> <li>- Fabric: Port 8-11 and port 20-17.</li> <li>- PCI-Express: port 4-7</li> </ul>
6.4	<b>AdvancedMC lane mapping</b>	AdvancedMC lane mapping shall be carefully selected so that full compatibility between ATCA and	Recommended port map according to SCOPE AMC port map gap analysis.

		MicroTCA is achieved.	
<b>6.5</b>	<b>Clocks</b>	<p>If required AdvancedMC must support relevant FCLK, TCLKA, TCLKB, TCLKC and TCLKD as per AdvancedMC specification.</p> <p>It is recommended that TCLK D is implemented as a “second” TCLKB.</p> <p>It is recommended that AdvancedMC implement a clock input selection mechanism to be future proof for a most probable change in the MicroTCA specification.</p>	<p><b>Gap (High Priority):</b> TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0.</p> <p><b>Gap (High Priority):</b> Selection of redundant clock input is not described in the AMC.0 R2.0 or MicroTCA.0 R1.0.</p>
<b>6.6</b>	<b>Telecom Clocks (see also Table 1)</b>	Definition and use case of Telecom Clocks as follows:	<b>Gap (High Priority): Current state of AdvancedMC and MicroTCA specifications do not necessarily follow the SCOPE Alliance Port Mapping recommendations, definition and use of Telecom Clocks. These different views must converge.</b>
	<b>Telecom Clocks #1</b>	<p>Clock Use Model for MCG with backplane line in:</p> <p>TCLKA: Line In (From MCH1 or Carrier).</p> <p>TCLKB: 8KHz/19.44MHz (Out to MCH1 or Carrier).</p> <p>TCLKC: Line In (From MCH2).</p> <p>TCLKD: 8KHz (Out to MCH2 or Carrier).</p>	<p>Gets line in from backplane or Carrier and provides 1 clock to each MCH or Carrier.</p> <p>TCLKB has the 19.44 MHz option to ensure compatibility with AdvancedTCA carriers built to AdvancedMC.0 R2.0.</p>
	<b>Telecom Clocks #2</b>	<p>Clock Use Model for MCG with front line in:</p> <p>TCLKA: 19.44MHz (Out to MCH1).</p> <p>TCLKB: 8KHz/19.44MHz (Out to MCH1 or Carrier).</p> <p>TCLKC: 19.44MHz (Out to MCH2).</p> <p>TCLKD: 8KHz (Out to MCH2 or Carrier).</p>	<p>Provides 2 clocks to each MCH or Carrier.</p> <p>TCLKB has the 19.44 MHz option to ensure compatibility with AdvancedTCA carriers built to AdvancedMC.0 R2.0.</p>
	<b>Telecom Clocks #3</b>	<p>AdvancedMC w/Line Out:</p> <p>TCLKA: Either 19.44 MHz or 8 KHz (In-MCH1 or carrier).</p> <p>TCLKB: Line Out (to MCH1 or carrier).</p> <p>TCLKC: Either 19.44 MHz or 8 KHz (In-MCH2 or carrier).</p> <p>TCLKD: Line Out</p>	

		(to MCH2).	
	<b>Telecom Clocks #4</b>	AdvancedMC without clock recovery: TCLKA: 19.44MHz (From MCH1 or Carrier). TCLKB: 8KHz (In from MCH1). TCLKC: 8 KHz (In from MCH2 or Carrier). TCLKD: 19.44MHz (In from MCH2).	MCH1 and MCH2 to deliver asymmetric clocks to a given AdvancedMC.
	<b>Telecom Clocks #5</b>	AdvancedMC used in AdvancedTCA carriers: TCLKA: 19.44 MHz In. TCLKB: Line out. TCLKC: 8 KHz In. TCLKD: Application dependant (Out as a "second" TCLKB recommended).	The use case is shown here to facilitate interoperability of the same AdvancedMCs in MicroTCA and AdvancedTCA.
6.7	<b>Clock Switching</b>	AdvancedMCs are expected to monitor both redundant clocks and to select autonomously the one of highest quality when appropriate.	<b>Gap (High Priority): AdvancedMC specifications do not specify redundant Telecom Clocks. AdvancedMCs are expected to monitor both redundant clocks and to select autonomously the one of highest quality when appropriate.</b>
6.8	<b>External Clock References</b>	Two external clock reference inputs may be provided on MCG.	
6.9	<b>Fabric Clock</b>	For MicroTCA system which provides PCI-Express between AdvancedMC pairs, it seems logical that the root-complex AdvancedMC could be able to provide the clock directly to its peripheral pair in this usage case.  It is recommended that root-complex capable processor AdvancedMCs be capable of receiving and providing the PCI-Express Fabric Reference Clock to/from the FCLK signals. This will enable usage in point-to-point PCI-Express connections without a central Carrier/MCH-resident clock generator, and star/point-to-point connections where a central Carrier/MCH provides the clock.	<b>Gap (High Priority): AdvancedMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clock source (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH).</b>  <b>PCI-E AdvancedMC acting as root complex must be capable of both generating and receiving PCI-E clock, which implies that PICMG should undertake an AdvancedMC.1 ECR.</b>
6.10	<b>Star fabric types, protocols and topologies</b>	Dual star 1GbE required.  Optionally either dual star 10GbE XAUI or (exclusive) dual start	Port 0 and port 1

		<p>SRIO 4x.</p> <p>Optionally PCI-Express 4x connectivity.</p> <p>Optionally SAS/SATA.</p>	
<b>6.11</b>	<b>Preferred method of protection (lines modules)</b>	<p>Some line interfaces are simplex, others use 1+1 or N+K redundancy. Application dependant.</p> <p>Port 12 shall be used for Automatic Protection Switching (APS) for SONET/SDH optical AdvancedMC, but it could also prove useful in other applications in the future. Thus, SCOPE avoids conflicting with this usage in the recommendations.</p>	<p>It is noted that all of 12-15 could potentially be used as Inter-AdvancedMC Point-to-Point connectivity for MicroTCA. But it is also noted that restrictions on the number of ports in the Update Channel provided by PICMG 3.0 could limit the usefulness of wider connectivity in AdvancedMC (there are 5 ports in the ATCA Update Channel – most logically one [Port 12] per AdvancedMC in a 4x AdvancedMC configuration, plus one for the Carrier itself).</p>

## 7. REGULATORY

<b>7.1</b>	<b>Regulatory</b>	<p>As per AdvancedMC specification.</p> <p>Central office systems require NEBS Level 3.</p>	
<b>7.2</b>	<b>Acoustic Noise</b> (Only when relevant)	<p>For AdvancedMC that's adds acoustic noise more than caused by normal airflow.</p> <p>Acoustic noise measurements for 23°C ± 2°C and maximum acoustic between 23°C to 27°C must be provided.</p> <p>Must meet NEBS GR-63 Issue 3 criteria and ETSI 300 753 Class 3.1 (telecommunication equipment room - attended) noise limits.</p> <p>Measurements at 40°C ambient temperature and maximum load should be provided (not required to meet noise-level requirements).</p>	<p>Acoustic noise requirements are defined at the system level. Therefore, the acoustic noise level should be measured for a fully equipped 42U high rack equipped with AdvancedTCA chassis/carriers or MicroTCA chassis.</p> <p>The system-level performance can also be simulated using a full rack of the equipment being measured.</p>
<b>7.3</b>	<b>EMC</b>	<p>Goal for individual AMC boards, EMC Class B -6dB compliance.</p> <p>Based on Telcordia GR-1089-CORE; FCC parts 15, 22, and 24. Class B. CISPR 22 Class B.</p>	<p>Shelf is expected to meet class A minus 6dB in order to make provision for multi-shelf configuration and still meet class A at system level. Goal is Class B equivalent for standalone shelf.</p> <p>Tested in a known good standard chassis/carrier.</p> <ul style="list-style-type: none"> <li>• Telcordia GR-1089-CORE, Electromagnetic Compatibility and</li> </ul>

			Electrical Safety Generic Criteria for Network Telecommunication Equipment. • Telcordia GR-63-CORE NEBS Requirements: Physical Protection REQ 8.11 Equipment should consider the following: • ES 201 468 Electromagnetic compatibility and Radio spectrum Matters (ERM); Additional Electromagnetic Compatibility (EMC) requirements and resistibility requirements for telecommunications equipment for enhanced availability of service in specific applications.
7.4	<b>Ecology standard</b>	RoHS (6/6) is preferred.  WEEE compliance as appropriate.	Products intended for sale to the EU must be designed to satisfy the following directives: • RoHS • WEEE • EuP Directive 2005/32/EC of the European Parliament and the Council of July 6, 2005 establishing a framework for the setting of eco design requirements for energy-using products and amending Council Directive 92/42/EEC and Directives 96/57/EC and 2000/55/EC of the European Parliament and the Council.
7.5	<b>Reliability standards</b>	As per Telcordia GR-512...	
7.6	<b>Safety testing standard</b>	As per IEC 60950-1  As per AdvancedMC appendix C	

## 8. AVAILABILITY

8.1	<b>Serviceability</b>	Hot swap of AdvancedMC cards is required.  Co-dependent AdvancedMC cards preferred to be hot swappable (e.g. Processor AdvancedMC cards and connected HDD AdvancedMC cards.	<b>Gap (Medium Priority): AMC.0 R2 does not describe how co-dependent AdvancedMC cards perform hot-swap.</b>
8.2	<b>Mean Time To Repair (MTTR)</b>	As per GR-512.	
8.3	<b>Reliability</b>	Failure rate prediction (MTBF) per Telcordia SR332.	Issue 2 is preferred.
8.4	<b>Service Life</b>	Service life should be 10 years.	Perform a service life estimation analysis to calculate the hardware equipment service life (also called product or endurance life); NEPs and telephone

			service providers ask for at least 10 years for hardware equipment.
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<b>9. OTHER</b>			
<b>9.1</b>	<b>Diagnostic / Test</b>	Support for POST and remote and local online and offline test or diagnostic.  JTAG shall be supported with >98% fault coverage.	
<b>9.2</b>	<b>Operating environment</b>	CO - NEBS 3 compliant/ETSI (including back office equipment).  Both outdoor and CPE – Enterprise use is foreseen; however, not covered in this version of the profile.	
<b>9.3</b>	<b>Storage solutions</b>	Local storage: - Hard disk drive on-board - Hard disk drive on adjacent AdvancedMC.  SAS Hard disk drive preferred  Optional RAID 0, 1, or 0+1 configuration  Optional non-rotating media (interface open)	SAS with controller on PrAdvancedMC is preferred.
		Self-contained storage units, AdvancedMC, within subrack and in case of ATCA also within blade:  - Storage AdvancedMC using iSCSI over IP over Ethernet - Optional RAID 0, 1, or 0+1 configuration - Optional non-rotating media (interface open)	iSCSI over 10GbE preferred
<b>9.4</b>	<b>Hard disk drive</b>	Disk life expectancy should be at least 5 years of service: - Operating condition: 24/7; - Duty cycle: 100%  Environment: NEBS/ETSI central office	SAS with controller on PrAdvancedMC preferred.
<b>9.5</b>	<b>Dual access to storage</b>	Capability to support dual homing is preferred	

**Clock Table for Telecom Clocks and MCH Clocks**

Table 1 shows the Clock Table for Telecom Clocks (profile requirements 6.6)

**Table 1: AMC Clock Usage.**

Use Cases Clock Signal Names	MCG with Backplane or Front Line In *	AMC w/ Line Out	Non-clock Recovery AMC †	AMC Designed for Carriers
<b>TCLKA [MCH1]</b>	Line in (From MCH1/Carrier)	Either 19.44 MHz or 8KHz (In-MCH1)	19.44 MHz (In from MCH1)	19.44 MHz In
<b>TCLKB [MCH1]</b>	8KHz / 19.44MHz (Out to MCH1/Carrier)	Line Out (to MCH1)	8 KHz (In from MCH1)	Out (Line Out)
<b>TCLKC [MCH2]</b>	Line In (From MCH2)	Either 19.44MHz or 8 KHz (In-MCH2)	8KHz (In from MCH2)	8 KHz In
<b>TCLKD [MCH2]</b>	8KHz (Out to MCH2/Carrier)	Line Out (to MCH2)	19.44 MHz (In from MCH2)	Application dependant (Out (Line Out) recommended)

\* Always 8 KHz in Micro TCA environment. MCH generates 19.44 MHz internally.

† MCH1 and MCH2 have inverted outputs.

## 6. SUMMARY

The SCOPE Alliance AdvancedMC Working Group has identified 13 gaps in the AdvancedMC specification. These gaps are listed, according to their priorities, below. There are 10 High Priority gaps and 3 Medium Priority gaps.

### High Priority

- 6.1 AdvancedMC Port Mapping: Current state of AdvancedMC and MicroTCA specifications, as well as current AdvancedMC and MicroTCA backplane and MCH designs, do not necessarily follow the SCOPE Alliance Port Mapping recommendations. These different views must converge. Recommended port map in accordance with the SCOPE port map gap-analysis.
- 6.1 AdvancedMC Port Mapping: AMC.2 and AMC.4 could be inconsistently mapped, due to a recent change in AMC.2. Ensure AMC.2 and AMC.4 mappings are consistent. It is recommended that AMC.4 also provides the 1<sup>st</sup> SRIO port on 8-11, consistent with AMC.2.
- 6.1 AdvancedMC Port Mapping: XAUI/SRIO ports of AMC.2 and AMC.4 overlap the x4 PCI-Express ports of AMC.1 on AdvancedMC Ports 4-7. Due to the value of PCI-Express and the need for dual-star XAUI/SRIO capable AdvancedMC and AdvancedMC-based systems, it is recommended that AMC.4 and AMC.2 find a new location other than Ports 4-7 for their second XAUI and x4 SRIO ports.
- 6.1 AdvancedMC Port Mapping: TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0. It is recommended that MicroTCA.0 take the lead in clarifying TCLKD usage and dual-star redundant-clock architecture for dual-star MicroTCA. Whether AMC.0 would need “re-updated” based on that clarification would depend on the content incorporated into MicroTCA.0.
- 6.1 AdvancedMC Port Mapping: AMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clock source (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH). It is recommended that AMC.1 provide more explicit guidance on who provides the PCI-Express Fabric Reference Clock. Generally the Reference Clock will be provided by the ATCA Carrier or PCI-Express capable MCH on the AdvancedMC FCLK signals. However, this can be a single-point of failure or simply not provided in systems with point-to-point PCI-Express connectivity and without PCI-Express switching provided by the MCH. It is also recommended that root-complex capable processor AdvancedMCs be capable of receiving *and providing* the PCI-Express Fabric Reference Clock to/from the FCLK signals. This will enable usage in point-to-point PCI-Express connections without a central Carrier/MCH-resident clock generator, *and* star/point-to-point connections where a central Carrier/MCH provides the clock. In systems requiring high-availability, but only having PCI-Express connectivity point-to-point, it would be desirable that each root-complex AdvancedMC provides the clock to its peripheral AdvancedMC. Currently, the Carrier (the MCH in MicroTCA) can be a single-point-of-failure if it is the sole provider of the PCI-Express clock. This may be acceptable in many cases, but not in the case of dual-star MicroTCA with PCI-Express solely provided as an inter-AdvancedMC point-to-point interconnect.
- 6.5 Clocks: TCLKD usage and dual-star redundant-clock architecture for MicroTCA is not clearly defined in AMC.0 R2.0 or MicroTCA.0 R1.0.
- 6.5 Clocks: Selection of redundant clock input is not described in the AMC.0 R2.0 or MicroTCA.0 R1.0.
- 6.6 Telecom Clocks: Current state of AdvancedMC and MicroTCA specifications do not necessarily follow the SCOPE Alliance Port Mapping recommendations, definition and use of Telecom Clocks. These different views must converge.

- 6.7 Clock Switching: AdvancedMC specifications do not specify redundant Telecom Clocks. AdvancedMCs are expected to monitor both redundant clocks and to select autonomously the one of highest quality when appropriate.
- 6.9 Fabric Clock: AdvancedMC.1: There is no provision for PCI-Express reference clock being provided in scenarios where there is no centralized clock source (e.g. point-to-point topologies w/out a clock source on the Carrier/MCH). PCI-E AdvancedMC acting as root complex must be capable of both generating and receiving PCI-E clock, which implies that PICMG should undertake an AdvancedMC.1 ECR.

#### **Medium Priority**

- 2.1 Corporate Appearance: PICMG should rigorously specify a "blank canvas" for attributes associated with faceplates, etc. The specification should include EMC sealing interface, faceplate and ejector handle mounting and operation, common LED locations, and labeling areas..If there is no common approach, a supplier independent interchangeability of faceplates and handles is required. For this PICMG should rigorously specify; EMC sealing interface, faceplate and ejector handle mounting and operation, common LED locations, and labeling areas to make full interoperability possible.
- 5.1 AdvancedMC thermal requirement: Specification on high operation temperature range is missing: -Method to be defined in PICMG, for better specification, prediction and management of thermals, e.g. definition of minimum/maximum air impedance, inlet air temperature, inlet air temperature when stacking etc.
- 8.1 Serviceability: AMC.0 R2 do not describe how co-dependent AdvancedMC cards perform hot-swap.